**(i) Explain in a brief paragraph, or two, the project developments that have taken place between September 2010-March 2011**

In this project, we have proposed an efficient algorithm to compute the topological similarities between two circuits. We have applied the proposed algorithm to Field Programmable Gate Array (FPGA) placement process, one of the most time consuming Computer Aided Design (CAD) phases for FPGAs, and we achieved significantly speedup (31X on average and up to 100X) with comparable or better quality compared to the state-of-the-art VPR placer.

Meanwhile, we have developed a circuit similarity-based placement toolset, including a circuit similarity placement tool and a circuit similarity visualization tool. The circuit similarity placement tool is developed under Linux with a command line user interface. The tool is able to convert logic level circuits into graphs, compute the topological similarities between the graphs and generate an initial placement for the new circuit. Therefore, the new circuit can be placed and routed significantly faster based on the highly optimized initial placement. The circuit similarity visualization tool is developed under Microsoft Windows with a user-friendly graphic user interface. The tool allows users to view the topological structures of a circuit (represented as a graph), and find the similar nodes between two graphs interactively. Two snapshots of the running program are attached.

We have so far published two conference papers and submitted one journal paper under review. Moreover, we are filing a U.S. patent in collaboration with TEC Edmonton. With the help from people in Intel, we are actively looking for CAD and FPGA companies that are interested in our invention.

**(ii) Note any publications or Reports on Inventions that are a direct result of the research from this project**

In summary, from this project, we have so far achieved the following:

- 1 paper has been published in the International Conference on Field-Programmable Technology (FPT), 2010;

- 1 paper has been published in The International Symposium on Quality Electronic Design (ISQED), 2011;

- 1 journal paper has been submitted to the Integration, the VLSI Journal;

- 1 report of inventions has been filed in collaboration with TEC Edmonton;

- 1 open-source circuit similarity-based placement toolset is developed, including a circuit similarity placement tool and a circuit similarity visualization tool.