CMPUT 329 - Computer Organization and Architecture II
Quiz # 6 — Fall 2003

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Name: **Solution**

CMPUT 329 Honor Code

By turning in the quiz solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2003/2004 Calendar.

Edmonton, December, 2003.

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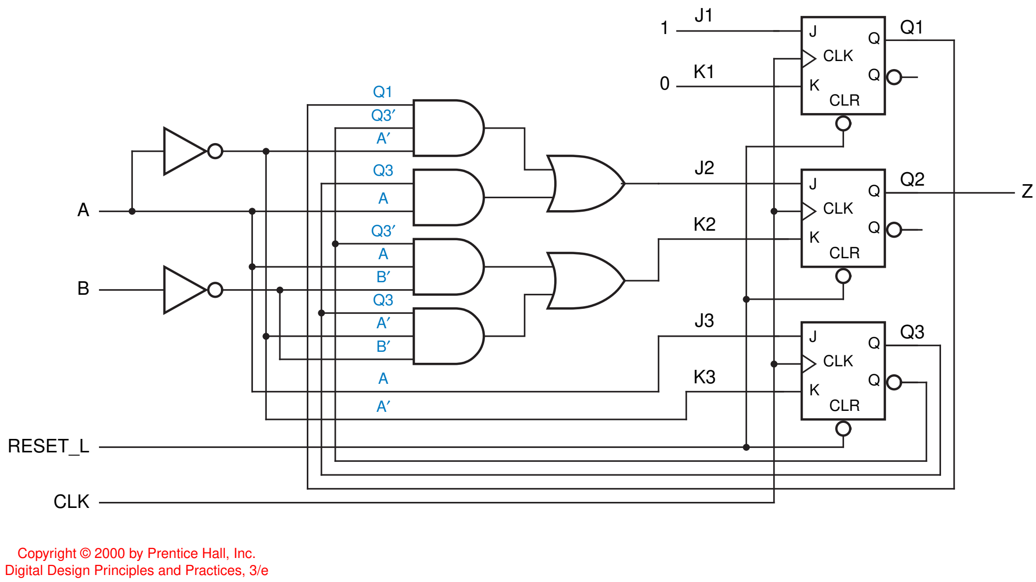


Figure 1: Logic Diagram for a finite state machine.

Question 1 (points):

Figure 1 shows a sequential circuit that implements a finite state machine with five states.

For this question, it might be useful to recall the Application table for J-K flip-flops that is presented on page 577 of your textbook:

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

This table provides the values that you have to have in the inputs J and K of the J-K flip-flop when you want to effect a transition from the current state Q to the next state Q+. An X in the table indicates a don't care.

a. (20 points) The following table contains one row for each of the JK flip-flop inputs, and one column for each combination of inputs into the sequential circuit. Write, in each entry of the table, the logic equation that makes the input in the row true for the combination of A and B specified in the column. For example, examining the circuit of Figure 1 we conclude that when `A=0` and `B=0`, then `J2` for `Q1 Q3'`, thus we write this boolean equation in the table.

JK Flip-Flop Inputs	Values of `A` and `B`			
	A=0 & B=0	A=0 & B=1	A=1 & B=0	A=1 & B=1
J2	Q1 Q3'	Q1 Q3'	Q3	Q3
K2	Q3	0	Q3'	0
J3	0	0	1	1
K3	1	1	0	0

b. (20 points) Complete the following transition and output table for the circuit of Figure 1.

Current State	Next State				Output
Q1 Q2 Q3	A=0 & B=0	A=0 & B=1	A=1 & B=0	A=1 & B=1	Z
000	100	100	101	101	0
001	100	100	111	111	0
010	110	110	101	111	1
011	110	110	111	111	1
100	100	110	101	101	0
101	110	100	111	111	0
110	110	110	101	111	1
111	100	110	111	111	1

State	Assignment Q1 Q2 Q3
INIT	000
A0	100
A1	101
OK0	110
OK1	111

Table 1: State Assignment for the sequential circuit of Table 2.

Current State	Next State				Output
	A=0 & B=0	A=0 & B=1	A=1 & B=0	A=1 & B=1	Z
INIT	A0	A0	A1	A1	0
A0	OK0	OK0	A1	A1	0
A1	A0	A0	OK1	OK1	0
OK0	OK0	OK0	A1	OK1	1
OK1	A0	OK0	OK1	OK1	1

Table 2: State Table a the sequential circuit.

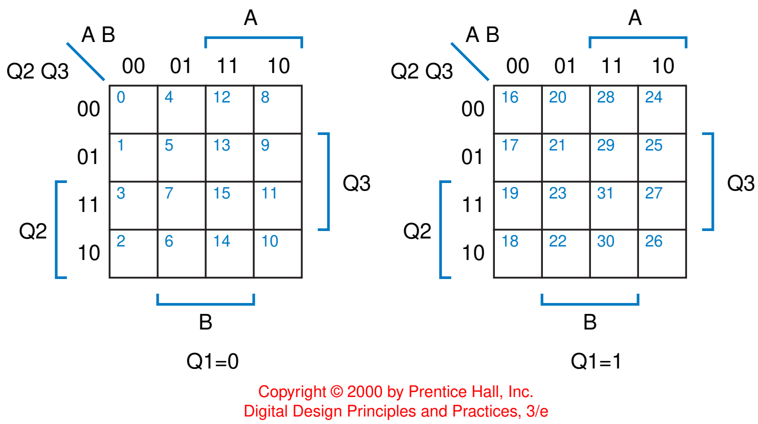
Question 2 (60 points): Table 2 shows the state transition diagram for a finite state machine. A state assignment for this finite state machine is shown in Table 1.

a. (10 points) You are asked to design a circuit that implements the finite state machine specified in Table 2 using D flip-flops. Using the state assignment of Table 1, complete the state transition table in Table 3.

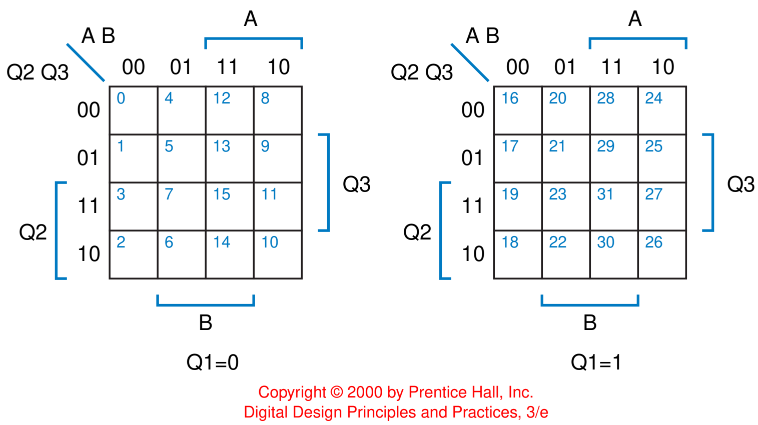
b. (20 points) Complete the Karnaugh Maps in Figure 2 with the values for D1, D2, and D3 based on the information on Table 3 (use don't cares for unused flip-flop combinations).

Current State	Next State				Output
	A=0 & B=0	A=0 & B=1	A=1 & B=0	A=1 & B=1	Z
Q1 Q2 Q3	Q1 Q2 Q3	Q1 Q2 Q3	Q1 Q2 Q3	Q1 Q2 Q3	
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	101	111	1
111	100	110	111	111	1

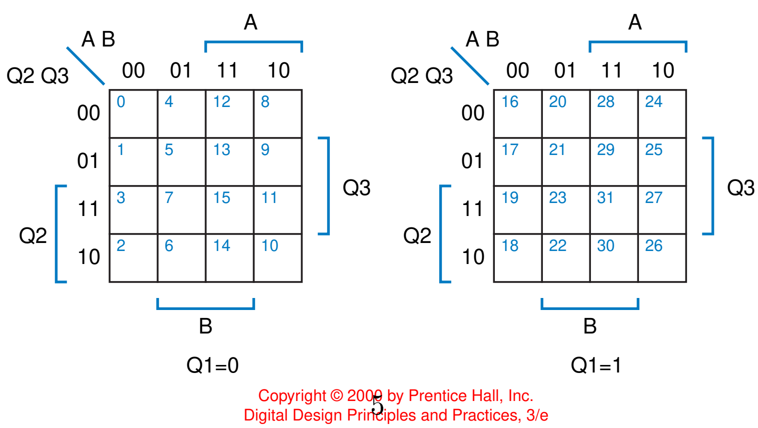
Table 3: State Transition Table for the sequential circuit of Table 3.



(a) Karnaugh Map for D1.



(b) Karnaugh Map for D2.



(c) Karnaugh Map for D3.

Figure 2: Karnaugh Maps for an implementation of the circuit of Figure 1 using D flip-flops.

c. (20 points) Write the minimized sum-of-product excitation equations for D1, D2, and D3, using the state assignment of Figure 1.

```
D1 = 1
D2 = Q1.Q3'.A' + Q3.A + Q2.B
D3 = A
```

d. (10 points) Assuming that you could interchange the circuit that you designed with the one shown in Figure 1. Is there a reason to prefer one circuit over the other? Explain.

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Not counting the inversors, the combinatorial portion of
the circuit of Figure 1 has a cost of 15.

Not counting the inversors, The combinatorial portion of
the circuit using D flip-flops has a cost of 7.

Both use the same number of flip-flops, thus from a cost
perspective, I would choose the D implementation.

The D implementation is also easier to design, and to test/degub.
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