CMPUT 329 - Computer Organization and Architecture II
Quiz # 1 — Fall 2003

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CMPUT 329 Honor Code

By turning in the quiz solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2002/2003 Calendar.

Edmonton, September, 2003.

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This is a **true** or **false** test. For each statement you have to indicate whether the statement is true or false. Use the capital letter T to indicate true, and the capital letter F to indicate false. You win 10 points for each correct answer. **You lose 5 points for each incorrect answer.** You are neither rewarded nor penalized for questions that you do not answer. If you answer all questions correctly you will make a maximum of 100 points. Regardless of how many questions you answer wrong, your score in the quiz cannot be below zero.

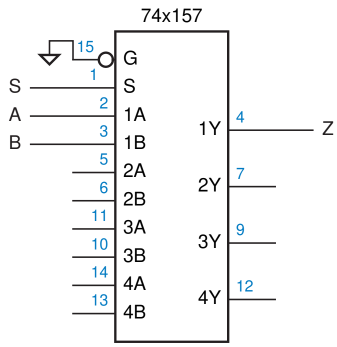

Figure 1: Block Diagram of a Digital Circuit

1. (**T**) If a digital circuit is properly designed, given the same set of inputs, it will always produce exactly the same results.

2. (**F**) Programmable logic makes the implementation of digital circuits less expensively, but it complicates the design.

3. (**F**) A very competent digital designer does not need to have very good troubleshooting skills because her designs will have no bugs.

4. (**T**) No special math skills are needed to master the skills involved in digital (or logic) design.

5. (**F**) A *flip-flop* is a digital device whose output constantly changes between 0 and 1.

6. (**F**) For military applications, manufacturers are required to design circuits that have the desired behavior under every possible condition of power-supply voltage, temperature, and loading.

7. (**T**) A well designed *test-bench* automatically exercises the function of a design and checks both its functional and its timing behavior.

8. (**F**) An *MCM* is a memory system formed by multiple cache memories.

9. (**T**) Figure 1 shows a multiplexer being used to implement a single logic equation with inputs S, A, and B.

10. (**F**) If a digital design written in HDL compiles correctly, it should work properly when downloaded to an FPGA.