CMPUT 329 - Computer Organization and Architecture II
Midterm Exam — Fall 2002

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Name:

CMPUT 329 Honor Code

By turning in the exam solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2001/2002 Calendar.

Edmonton, October 21, 2002.

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Question 1	/20
Question 2	/20
Question 3	/20
Question 4	/20
Question 5	/20
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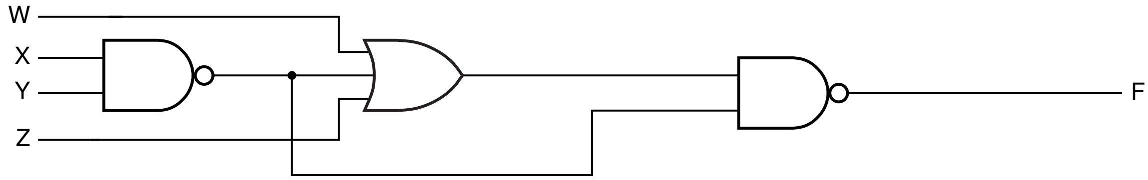

Figure 1: A combinatorial circuit for analysis

Question 1 (20 points):

For the circuit presented in Figure 1 you are asked to:

a. (5 points) Write the logic expression for the output F in terms of the inputs W, X, Y, and Z. Your expression for F should reflect the structure of the circuit, do not simplify.

b. (10 points) What is the cost of implementing this circuit (use the standard cost function that counts the number of gate inputs)?

c. (5 points) Now simplify F **algebraically**, indicating all the intermediary steps of your simplification, to generate a (at most) 2-level NAND-NAND expression. (Hint: When implementing a NAND-NAND circuit, the only gate type that you are allowed to use is NAND.)

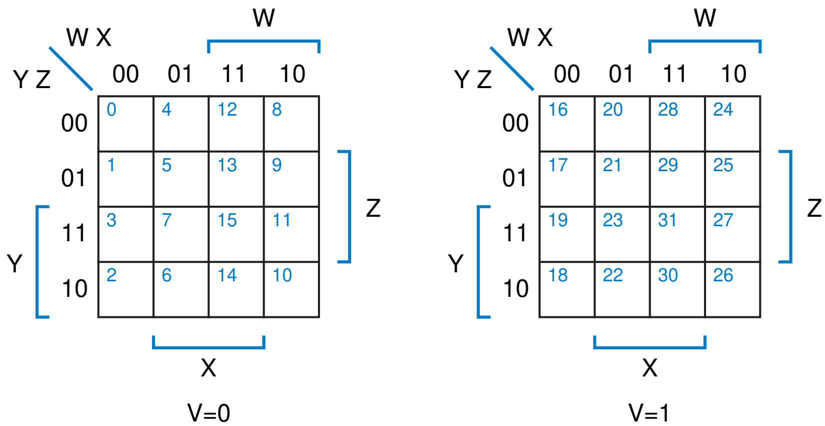

Figure 2: Karnaugh Map for $F(V,W,X,Y,Z)$ A combinatorial circuit for analysis

Question 2 (20 points):

During your first week working at *ACME Electronic Solutions* you are told that their PLA down-loader is not working. They need you to implement some small circuits that were originally designed using VHDL. Because PLAs are not available, you have to use discrete LSI logic gates to meet the deadline for testing an important product. One of the functions that you have to implement is the glue logic function F that was specified by the VHDL code below. Remember that in the std_logic type defined in the IEEE.std_logic_1164, `'-'` is the symbol used for don't care.

```
entity gluefunc is
  port (V, W, X, Y, Z: in STD_LOGIC;
        F:             out STD_LOGIC);
end gluefunc
architecture gluefunc_arc of gluefunc is
begin
  F <= '1' when (V='0' and W='0' and X='0') else
       '1' when (V='0' and X='0' and Y='0') else
       '1' when (V='1' and W='1' and Y='0' and Z='0') else
       '1' when (V='1' and W='0' and X='0' and Y='1') else
       '-' (when X='1' and Y='1')
       else '0';
end gluefunc_arc
```

a. (10 points) Fill the Karnaugh Map of Figure 2 using the values specified for the function $F(V,W,X,Y,Z)$ in the VHDL code.

b. (5 points) What is the cost of a minimal sum-of-products implementation of this function (assume that both the input signals and their complements are already available)?

c. (5 points) What is the cost of the implementation if you have to ensure that there is no static-1 hazard(assume that both the input signals and their complements are already available)?

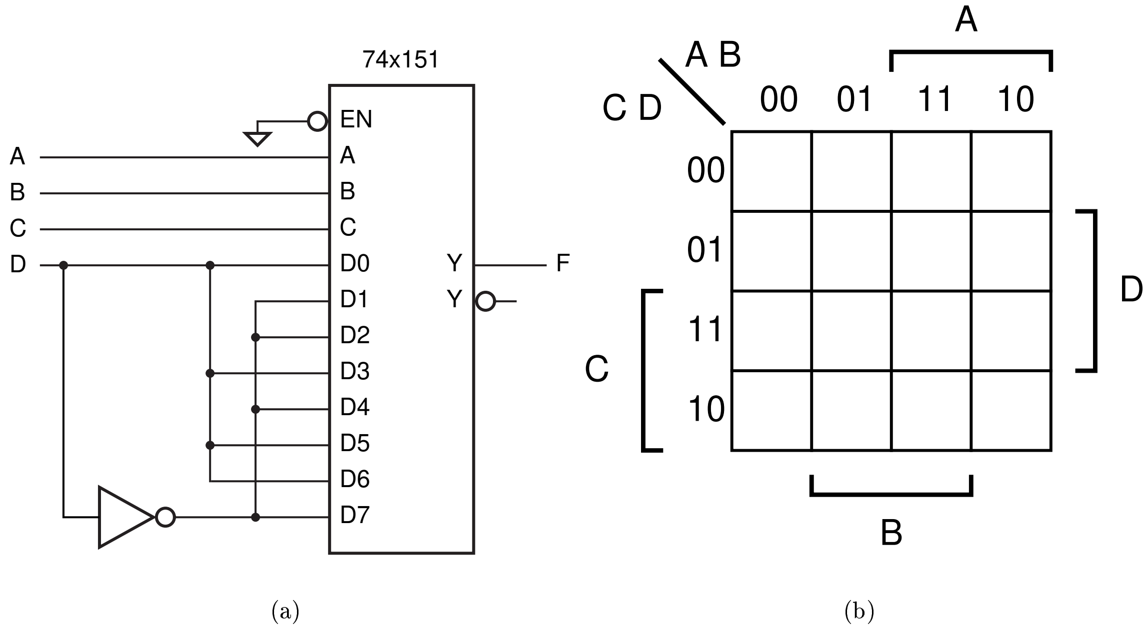

Figure 3: (a) A multiplex that implements a combinatorial function; (b) Karnaugh Map

Question 3 (20 points):

The 74x151 shown in Figure 3(a) is an 8-to-1 multiplex that is being used to implement a combinatorial function $F(A, B, C, D)$.

a. (10 points) Fill the Karnaugh map of Figure 3(b) with the logic function $F(A, B, C, D)$ that is realized by the circuit of Figure 3(a). (Hint: When numbering the control inputs of the 74x151, C is the most significant bit, and A is the least significant bit.)

b. (10 points) Using only XOR gates, draw a minimized logic diagram that implements the same function.

Question 4 (20 points):

The circuit presented in Figure 4 is used in a microprocessor system as an address decoder to chip-select various memories and peripherals. The microprocessor has 16 address bits, $A[15:0]$ that enable it to specify a 64 Kbyte address space, hex addresses `0000-FFFF`. Fill the table below the figure with the values of A15-A8 that will make each of the chip select signals active. Use 'x' to indicate that the chip select will be active when the input in the column is either 0 or 1. (Hint: Notice that all the chip select signals are active low.) To assist you, we present the internal circuit diagram of the 3-to-8 74x138 decoder in Figure 5.

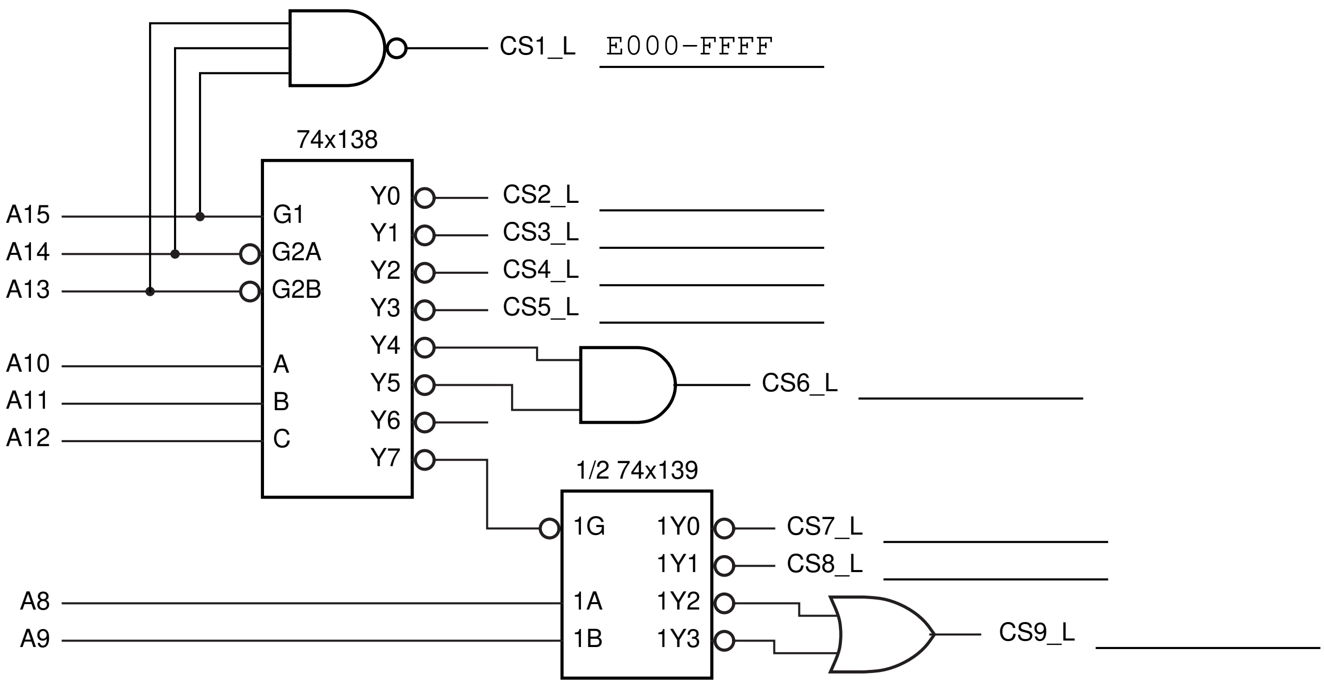

Figure 4: Address Decodification Circuit for a Memory System.

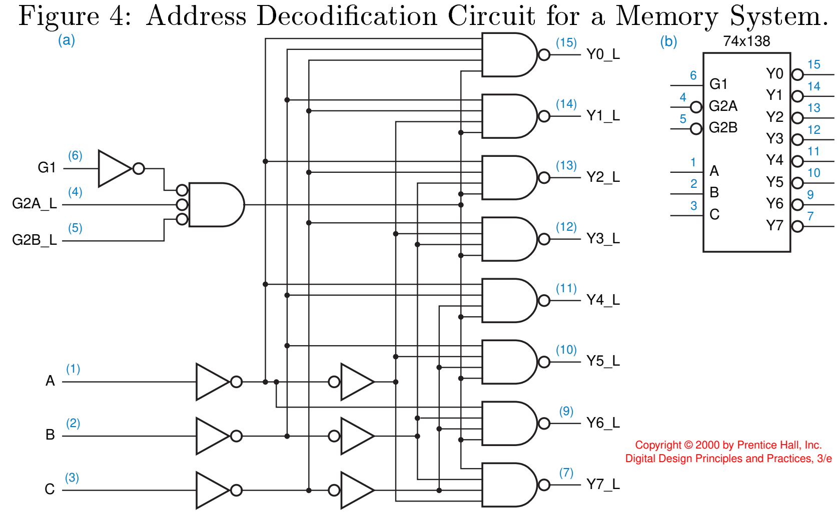

Figure 5: Internal Circuit of the 74x138 3-to-8 decoder.

A15	A14	A13	A12	A11	A10	A9	A8	CS1_L	CS4_L	CS6_L	CS7_L	CS8_L	CS9_L
1	1	1	x	x	x	x	x	0	1	1	1	1	1
								1	0	1	1	1	1
								1	1	0	1	1	1
								1	1	1	0	1	1
								1	1	1	1	0	1
								1	1	1	1	1	0

Product	Minterms									
Term	m_1	m_3	m_4	m_5	m_7	m_9	m_{10}	m_{11}	m_{12}	m_{14}
P_a	x	x				x		x		
P_b	x	x		x	x					
P_c			x	x						
P_d			x						x	
P_e							x	x		
P_f							x			x
P_g									x	x

Table 1: Prime implicant chart for $F(x, y, w, z,)$

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Question 5 (20 points): Table 1 presents the prime implicant table for function $F(x, w, y, z)$.

a. (10 points) In the table below list all the essential prime implicants of $F(x, w, y, z)$ and their expression in terms of x, w, y, z. (Hint: When numbering the minterms, x is the most significant bit, and z is the least significant bit.)

Product Term	**Expression**

b. (10 points) Write a minimum product of sums form for $F(x, w, y, z)$. What is the implementation cost of $F(x, w, y, z)$?