CMPUT 329 - Computer Organization and Architecture II
Midterm Exam — Fall 2001

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Name:

CMPUT 329 Honor Code

By turning in the exam solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2001/2002 Calendar.

Edmonton, October 22, 2001.

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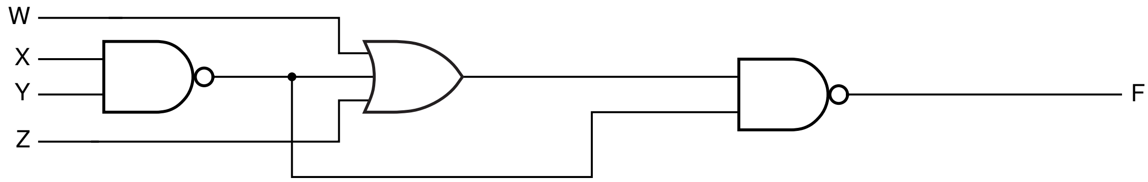


Figure 1: A combinatorial circuit for analysis

Question 1 (20 points):

For the circuit presented in Figure 1 you are asked to:

a. (5 points) Write the logic expression for the output F in terms of the inputs W, X, Y, and Z. Your expression for F should reflect the structure of the circuit, do not simplify.

b. (5 points) What is the cost of implementing this circuit?

c. (5 points) Now simplify F **algebraically**, indicating all the intermediary steps of your simplification, to generate a (at most) 2-level NAND-NAND expression.

d. (5 points) What is the cost of implementing the circuit **after** your algebraic simplification (assume that the complement of the input signals are not available, but the cost of each NAND is equal the number of inputs in the NAND gate)?

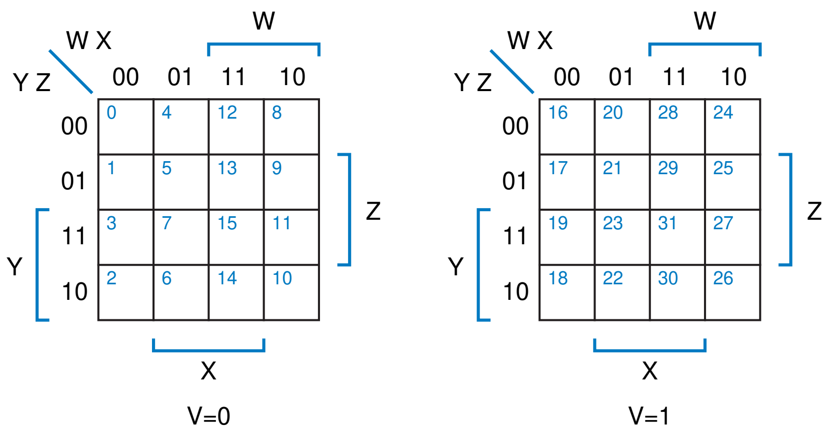


Figure 2: Karnaugh Map for $F(V, W, X, Y, Z)$ A combinatorial circuit for analysis

Question 2 (20 points):

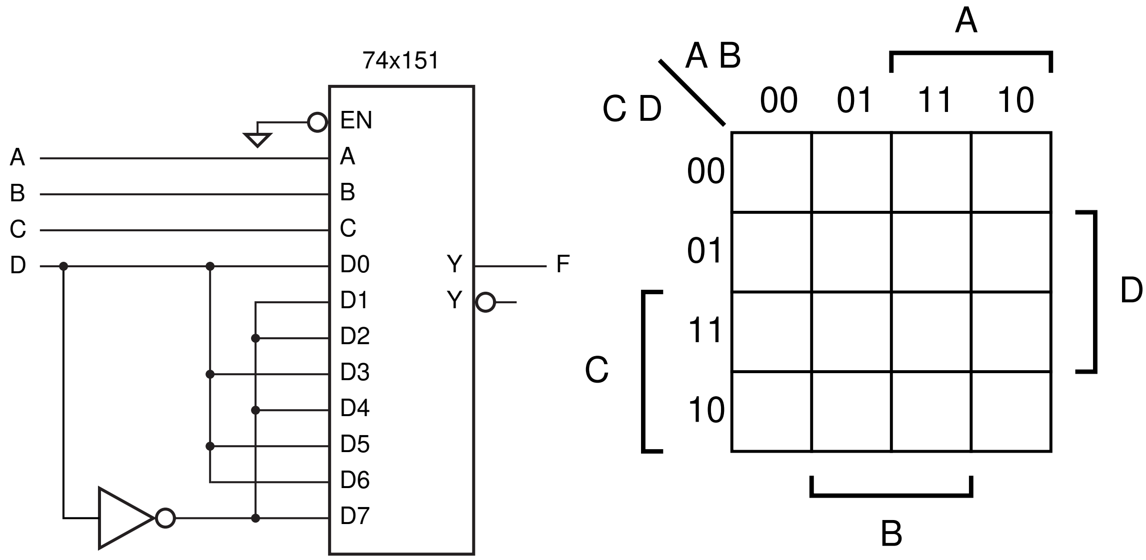
During your first week working at *ACME Electronic Solutions* you are told that their PLA down-loader is not working. They need you to implement some small circuits that were originally designed using VHDL. Because PLAs are not available, you have to use discrete LSI logic gates to meet the deadline for testing an important product. One of the functions that you have to implement is the glue logic function F that was specified by the VHDL code below. Remember that in the std_logic type defined in the IEEE.std_logic_1164, `'-'` is the symbol used for don't care. In the Karnaugh Map of Figure 1(b):

```
entity gluefunc is
  port (V, W, X, Y, Z: in STD_LOGIC;
        F:             out STD_LOGIC);
end gluefunc
architecture gluefunc_arc of gluefunc is
begin
  F <= '1' when (V='0' and W='0' and X='0') else
       '1' when (V='0' and X='0' and Y='0') else
       '1' when (V='1' and W='1' and Y='0' and Z='0') else
       '1' when (V='1' and W='0' and X='0' and Y='1') else
       '-' (when X='1' and Y='1')
       else '0';
end gluefunc_arc
```

a. (10 points) Fill the Karnaugh Map of Figure 2 using the values specified for the function $F(V, W, X, Y, Z)$ in the VHDL code.

b. (5 points) What is the cost of a minimal sum-of-products implementation of this function (assume that both the input signals and their complements are already available)?

c. (5 points) What is the cost of the implementation if you have to ensure that there is no static-1 hazard(assume that both the input signals and their complements are already available)?



(a) (b)

Figure 3: (a) A multiplex that implements a combinatorial function; (b) Karnaugh Map

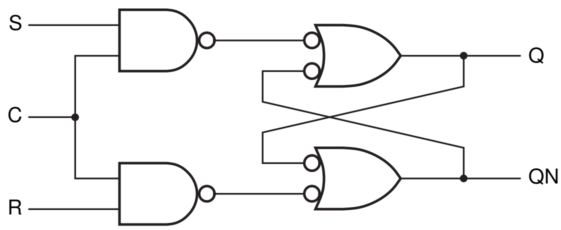
Question 3 (20 points):

The 74x151 shown in Figure 3(a) is an 8-to-1 multiplex that is being used to implement a combinatorial function $F(A, B, C, D)$.

a. (10 points) Fill the Karnaugh map of Figure 3(b) with the logic function $F(A, B, C, D)$ that is realized by the circuit of Figure 3(a).

b. (10 points) Using only XOR gates, draw a minimized logic diagram that implements the same function.

(a)



(b)

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

(c)

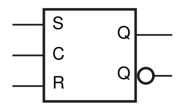


Figure 4: S-R latch with enable input; (a) circuit using NAND gates, (b) function table; (c) logic symbol

Question 4 (20 points):

Figure 4 shows the circuit for an S-R latch with C enable input.

a. (10 points) Draw, in the figure, the changes that you need to do to this circuit in order to obtain a D latch with a C enable input.

b. (10 points) In the space below, draw the function table for the D latch that you created with your circuit modifications in the picture.

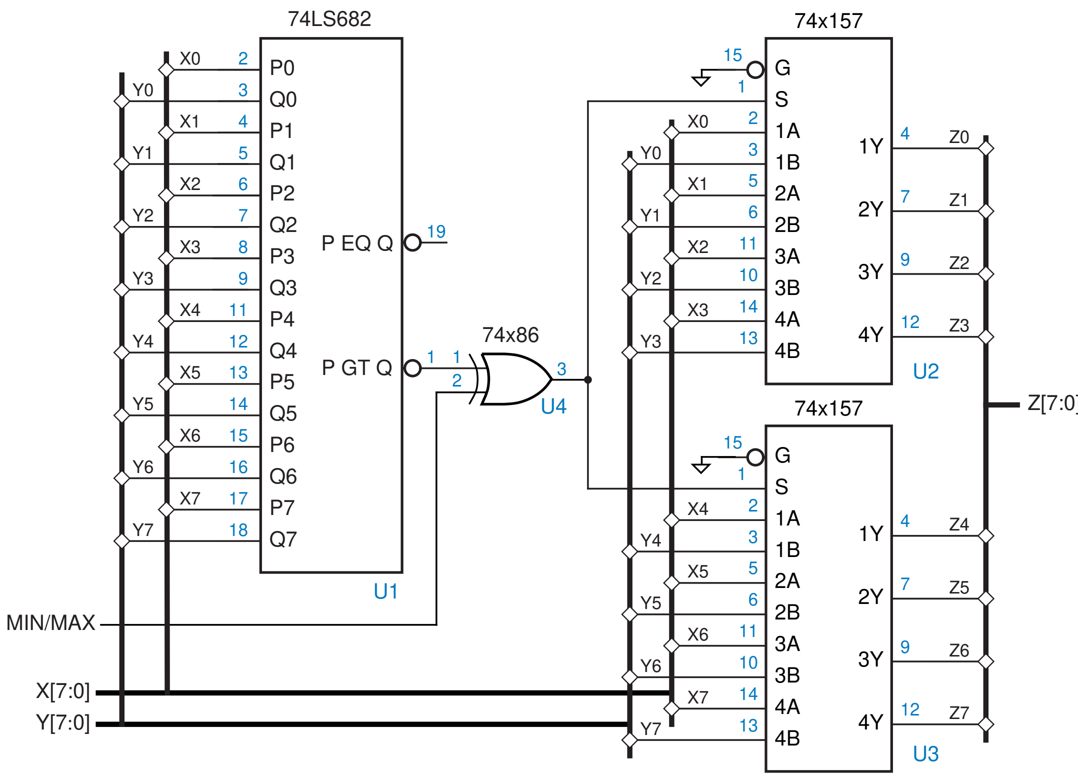


Figure 5: Combinatorial Circuit for Time Analysis

Question 5 (20 points):

For the combinatorial circuit of Figure 5, assume that all circuits are 74LS, and use the delays for the 2 level version of the 74LS86. Using the Tables of Figures 6 and 7, and :

a. (10 points) Determine the <u>**maximum**</u> propagation delay from a transition on the MIN/MAX input to a change in the Z output.

b. (10 points) Determine the <u>**maximum**</u> propagation delay from a transition on the X input to a change in the Z output.

Table 5-2 Propagation delay in nanoseconds of selected 5-V CMOS and TTL SSI parts.

	74HCT		*74AHCT*				*74LS*			
	Typical	*Maximum*	*Typical*		*Maximum*		*Typical*		*Maximum*	
Part number	t_{pLH}, t_{pHL}	t_{pLH}, t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
'00, '10	11	35	5.5	5.5	9.0	9.0	9	10	15	15
'02	9	29	3.4	4.5	8.5	8.5	10	10	15	15
`04	11	35	5.5	5.5	8.5	8.5	9	10	15	15
'08, '11	11	35	5.5	5.5	9.0	9.0	8	10	15	20
'14	16	48	5.5	5.5	9.0	9.0	15	15	22	22
'20	11	35	9	10	15	15				
'21	11	35	8	10	15	20				
'27	9	29	5.6	5.6	9.0	9.0	10	10	15	15
'30	11	35	8	13	15	20				
'32	9	30	5.3	5.3	8.5	8.5	14	14	22	22
'86 (2 levels)	13	40	5.5	5.5	10	10	12	10	23	17
'86 (3 levels)	13	40	5.5	5.5	10	10	20	13	30	22

Figure 6: Propagation delay in nanoseconds of selected 5-V CMOS and TTL SSI parts

Table 5-3 Propagation delay in nanoseconds of selected CMOS and TTL MSI parts.

			74HCT		74AHCT / FCT		74LS			
			Typical	Maximum	Typical	Maximum	Typical		Maximum	
Part	**From**	**To**	t_{pLH}, t_{pHL}	t_{pLH}, t_{pHL}	t_{pLH}, t_{pHL}	t_{pLH}, t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
'138	any select	output (2)	23	45	8.1 / 5	13 / 9	11	18	20	41
	any select	output (3)	23	45	8.1 / 5	13 / 9	21	20	27	39
	$\overline{G2A}$, $\overline{G2B}$	output	22	42	7.5 / 4	12 / 8	12	20	18	32
	G1	output	22	42	7.1 / 4	11.5 / 8	14	13	26	38
'139	any select	output (2)	14	43	6.5 / 5	10.5 / 9	13	22	20	33
	any select	output (3)	14	43	6.5 / 5	10.5 / 9	18	25	29	38
	enable	output	11	43	5.9 / 5	9.5 / 9	16	21	24	32
'151	any select	Y	17	51	- / 5	- / 9	27	18	43	30
	any select	$\overline{Y}$	18	54	- / 5	- / 9	14	20	23	32
	any data	Y	16	48	- / 4	- / 7	20	16	32	26
	any data	$\overline{Y}$	15	45	- / 4	- / 7	13	12	21	20
	enable	Y	12	36	- / 4	- / 7	26	20	42	32
	enable	$\overline{Y}$	15	45	- / 4	- / 7	15	18	24	30
'153	any select	output	14	43	- / 5	- / 9	19	25	29	38
	any data	output	12	43	- / 4	- / 7	10	17	15	26
	enable	output	11	34	- / 4	- / 7	16	21	24	32
'157	select	output	15	46	6.8/7	11.5/10.5	15	18	23	27
	any data	output	12	38	5.6 / 4	9.5 / 6	9	9	14	14
	enable	output	12	38	7.1/7	12.0/10.5	13	14	21	23
'182	any $\overline{Gi}$, $\overline{Pi}$	C1–3	13	41			4.5	4.5	7	7
	any $\overline{Gi}$, $\overline{Pi}$	$\overline{G}$	13	41			5	7	7.5	10.5
	any $\overline{Pi}$	$\overline{P}$	11	35			4.5	6.5	6.5	10
	C0	C1–3	17	50			6.5	7	10	10.5
'280	any input	EVEN	18	53	- / 6	- / 10	33	29	50	45
	any input	ODD	19	56	- / 6	- / 10	23	31	35	50
'283	C0	any Si	22	66			16	15	24	24
	any Ai, Bi	any Si	21	61			15	15	24	24
	C0	C4	19	58			11	11	17	22
	any Ai, Bi	C4	20	60			11	12	17	17
'381	CIN	any Fi			18	14	27	21		
	any Ai, Bi	$\overline{G}$			20	21	30	33		
	any Ai, Bi	$\overline{P}$					21	33	23	33
	any Ai, Bi	any Fi					20	15	30	23
	any select	any Fi			35	34	53	51		
	any select	$\overline{G}$, $\overline{P}$	31	32	47	48				
'682	any Pi	$\overline{PEQQ}$	26	69	- / 7	- / 11	13	15	25	25
	any Qi	$\overline{PEQQ}$	26	69	- / 7	- / 11	14	15	25	25
	any Pi	$\overline{PGTQ}$	26	69	- / 9	- / 14	20	15	30	30
	any Qi	$\overline{PGTQ}$	26	69	- / 9	- / 14	21	19	30	30

Figure 7: Propagation delay in nanoseconds of selected 5-V CMOS and TTL MSI parts