# CMPUT 329 - Computer Organization and Architecture II
# Midterm Exam — Fall 2000

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## CMPUT 329 Honor Code

By turning in the exam solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2000/2001 Calendar.

Edmonton, October 23, 2000.

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**Question 1 (20 points):** You are asked to design a circuit for a two bit multiplier, it takes as input, two two-bit numbers, $A$ and $B$, and produces as output one four-bit product $P$. You should call the inputs to your network $A_1$, $A_0$, $B_1$, and $B_0$. If $A_1 = 1$ and $A_0 = 1$, then $A = 3_{10}$. If $A_1 = 1$, and $A_0 = 0$, then $A = 2_{10}$, and so on so far The product $P$ is represented as $P_3P_2P_1P_0$, therefore if the product is $P = 6$, your circuit should produce $P_3 = 0$, $P_2 = 1$, $P_1 = 1$, and $P_0 = 0$.

a. Specify the truth table for a ROM which would realize this circuit.

b. What is the minimum size PLA that you could use to implement this circuit. The number of input and output lines in a PLA is determined by the problem, therefore you only can minimize the number of product term lines. How many product term lines you have to use? Show how you arrive at this number.

**Question 2 (20 points):** Now you are asked to implement a circuit that take as an input the product term $P$ produced by the circuit of the previous question, and that produces two outputs: $M_2$, and $M_3$. $M_2$ is true if and only if the $P$ is a multiple of 2, and $M_3$ is true if and only if $P$ is a multiple of 3. Notice that zero is a multiple of any integer number.

a. Use a Karnaugh map to obtain the minimal expressions for separate circuits that implement $M_2$ and $M_3$ (in this implementation $M_2$ and $M_3$ cannot share logic gates).

b. Use the definition for the cost of an expression given in class to compute the costs of implementing $M_2$ and $M_3$.

**Question 3 (20 points):** The Quine-McCluskey method generates the following prime implicant chart for a function $F(A, B, C, D, E)$

| | 00 | 02 | 03 | 05 | 07 | 09 | 11 | 13 | 14 | 16 | 18 | 24 | 26 | 28 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B'C'E' | X | X | | | | | | | | X | X | | | | |
| AB'E' | | | | | | | | | | X | X | X | X | | |
| ABE' | | | | | | | | | | | | X | X | X | X |
| A'B'C'D | | X | X | | | | | | | | | | | | |
| A'B'DE | | | X | | X | | | | | | | | | | |
| A'C'DE | | | X | | | | X | | | | | | | | |
| A'B'CE | | | | X | X | | | | | | | | | | |
| A'CD'E | | | | X | | | | X | | | | | | | |
| A'BC'E | | | | | | X | X | | | | | | | | |
| A'BD'E | | | | | | X | | X | | | | | | | |
| BCDE' | | | | | | | | | X | | | | | | |

Write a minimal form for the function $F(A, B, C, D, E)$.

**Question 4 (20 points):** Implement the function f(a,b,c) = ab'c' + a'bc'+ bc using a 4-to-1 multiplexer.

**Question 5 (20 points):** The Set-Reset flip-flop (S-R) is built with two NOR gates. When $S = R = 0$, its next state is identical to the current state. If $S = 1$ and $R = 0$, the next state is set, i. e., $Q = 1$ and $Q' = 0$. If $S = 0$ and $R = 1$, the next state is reset, i. e., $Q = 0$ and $Q' = 1$. However when both $S = 1$ and $R = 1$, the next state is undetermined. You are asked to design a **set dominant S-R flip-flop**. This flip-flop should behave exactly like the S-R flip-flop, except that when both $S = 1$ and $R = 1$, the next state must be $Q = 1$, and $Q' = 0$. Use the minimum number of gates to design your flip-flop.