CMPUT 329 - Computer Organization and Architecture II
Final Exam — Fall 2002

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Name:

CMPUT 329 Honor Code

By turning in the exam solution for grading, I certify that I have worked all the solutions on my own, that I have not copied or transcribed solutions from a classmate, someone outside the class, or from any other source. I also certify that I have not facilitated or allowed any of my classmates to copy my own solutions. I am aware that the violation of this honor code constitutes a breach of the trust granted me by the teaching staff, compromises my reputation, and subjects me to the penalties prescribed in Section 26.1 of the University of Alberta 2001/2002 Calendar.

Edmonton, December 12, 2002.

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Question 1	/20
Question 2	/20
Question 3	/20
Question 4	/20
Question 5	/20
Total	/100
Curving	/100
Rank	/

Q1Q2Q3	State	Q1Q2Q3	State
000	A	100	E
001	B	101	F
010	C	110	G
011	D	111	H

Table 1: State Assignment for the state machine of Figure 1.

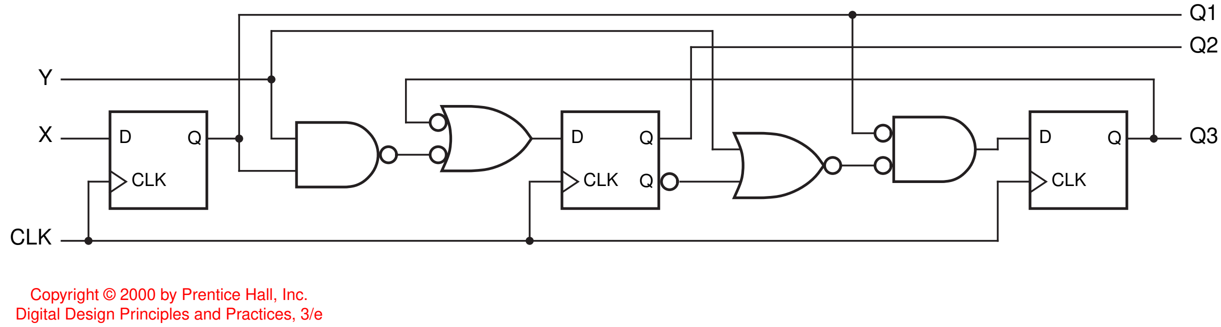


Figure 1: Circuit to Implement a Finite State Machine.

Question 1 (20 points): Analysing a Sequential Design

Figure 1 displays the implementation of a clocked synchronous state machine. When reading the value of a state use the state the state assignment shown in Table 1.

a. (**10 points**) Complete the state transition table in Table 2 with the correct value of each state based on the circuit in Figure 1.

b. (**10 points**) Write the excitation equations for each one of the flip flops in Figure 1.

Current State	Next State			
	X=0 & Y=0	X=0 & Y=1	X=1 & Y=0	X=1 & Y=1
A				
B				
C				
D				
E				
F				
G				
H				

Table 2: State Transition Table for machine of Figure 1.

Part	From	To	Typical		Maximum	
			t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
74LS138	any select	output	11	18	20	41
	G2A, G2B	output	12	20	27	39
	G1	output	14	13	26	38
74LS139	any select	output	13	22	20	33
	enable	output	14	13	26	38

Table 3: Propagation delay in nanoseconds for some TTL MSI parts.

Question 2 (20 points): Cascading Decoders

Figure 2 shows a 5-to-32 decoder built through the cascading of four 74x138s combined with one 74x139. Analyse the circuit and respond the following questions.

a. **5 points**) What values should the inputs `EN1`, `EN2_L`, and `EN3_L` have in order for any of the outputs to be active?

b. (**5 points**) Which outputs may be active if we have `N1 = 1`, `N2 = 1`, `N3 = 0`, and `N4 = 1`.

c. (**5 points**) Is it possible for `DEC16_L` and `DEC25_L` to be 0 at the same time? Explain your answer.

d. (**5 points**) The propagation delay provided by the manufacturer for the 74LS138 and for the 74LS139 are shown in Table 3. What is the maximum propagation delay that you should expect from the transition of a single input of the circuit in Figure 2 until all outputs are stable?

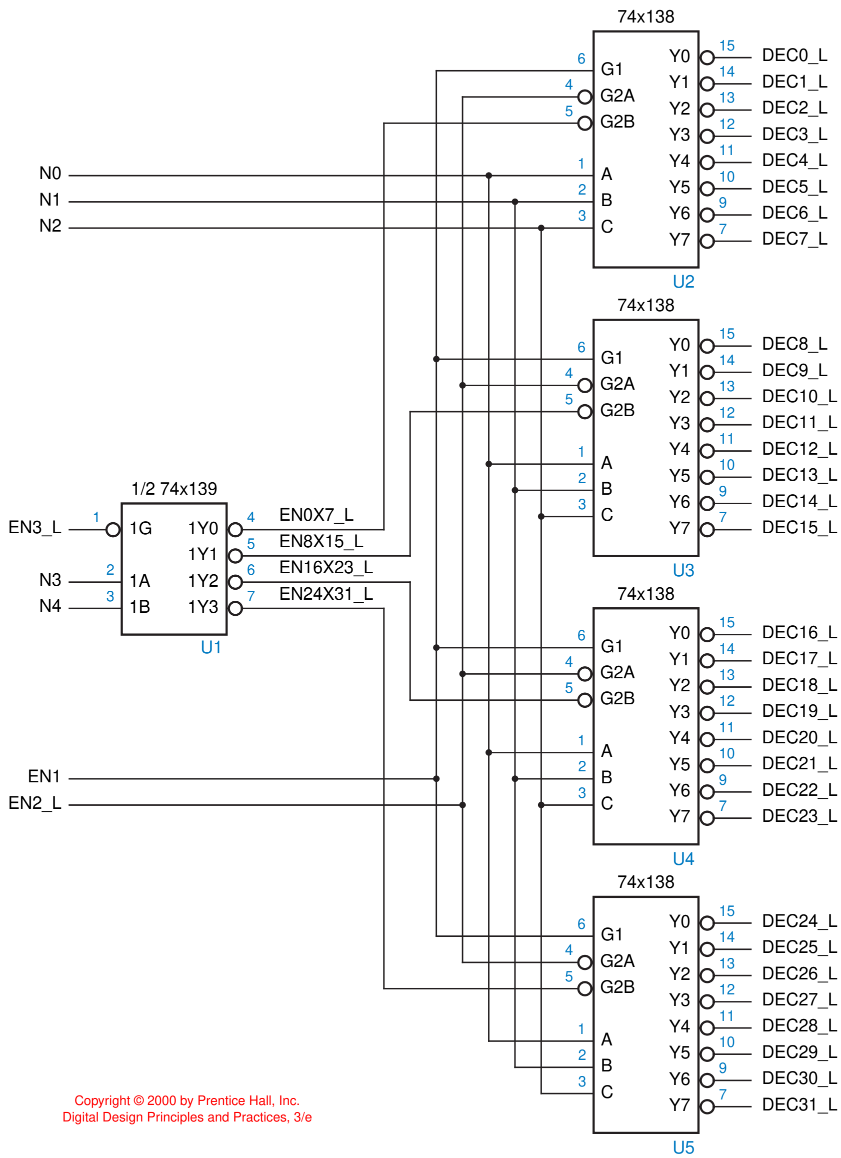


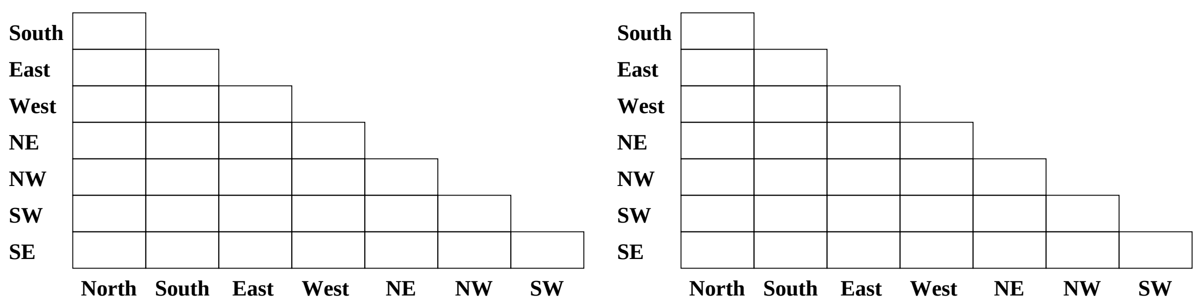
Figure 2: Circuit to Implement a Finite State Machine.

Current State	Next State		Outputs	
	Go = 0	Go = 1	Light	Beep
North	West	SW	0	0
South	SE	East	1	1
East	NE	North	0	1
West	East	South	1	0
NW	NE	NW	1	1
SW	West	South	0	0
NE	East	NW	1	0
SE	SE	East	0	1

Table 4: State Transition Table for the Spacecraft Controller.

Question 3 (20 points): State Assignment: A Cheater's Dilemma

During final exams Steve is trying to solve a question that asks the students to finish the design of a controller for a spacecraft in a video-game. This controller has one input, Go, and two outputs, Light and Beep. The students were presented with the state transitions and outputs shown in Table 4 for the finite state machine.



(a) Successor DAG (b) Predecessor DAG

Figure 3: (a) Successor DAG; (b) Predecessor DAG.

The students were asked to create the Successor Desired Adjacency Graph (DAG), and the Predecessor DAG for this finite state machine. Fortunately Steve remembers from the lectures that the successor, predecessor, and output rules are stated as follows:

Successor Rule: The next states of a given state should be close to each other.

Predecessor Rule: States that have the same next state for a given input should be close to each other.

Output Rule: States that have the same output should be close to each other.

(a) (**5 points**) Knowing these rules, how would Steve have completed the values in each edge of the DAGs in Figure 3?

Steve also remembers that the predecessor rule is the most important one, followed by the successor rule, and then by the output rule. The exam question continues by asking the students to

John's Assignment	
State	**Code**
North	000
South	111
East	010
West	101
NW	011
SW	100
NE	001
SE	110

(a) John's Solution

Tim's Assignment	
State	**Code**
North	000
South	001
East	101
West	111
NW	011
SW	010
NE	100
SE	110

(b) Tim's Solution

Figure 4: State Assignments from John and Tim that Steve "accidentally" saw.

find a good state assignment and to produce the minimal equations for the D flip-flops excitation and for the outputs. Unfortunately Steve slept through that portion of the class and did not review the class slides. Thus he has no idea how to perform the state assignment. However Steve "accidentally" saw that John, the student to his left, and Tim, the student to his right, have chosen the assignments shown in Figure 4. The exam is a long one. Steve knows that he does not have time to do the five four-input equation minimizations for each assignment to decide which assignment to use.

(b) (**10 points**) Should Steve choose to use John's or Tim's assignment for his solution? Without generating and minimizing the equations, provide a very convincing explanation for this choice. (Hint: to analyze John's and Tim's solutions, you might want to either build state distance graphs, or to place the states into a Karnaugh Map according to their assignments.)

(c) (**5 points**) If Steve is concerned about being caught cheating, what changes could he do to the assignment so that it looks different from the one that he copied? Steve wants to make changes that make his assignment look different so that he is not caught cheating by the grader, but he does not want these changes to affect the cost of the equations that are produced.

Question 4 (20 points): Improving a design

The company that you are consulting for fabricates all kinds of small knick-knacks. One of them is a keychain with a led and a button. Because they plan to sell millions of keychains, it is very important that the circuit be minimized. They need to design a state machine with one input and one output. One of their engineers has completed the design of the state machine using D flip-flops, and has provided you with the following excitation equations (the input is called I and the output is called W):

$$\begin{aligned} Q_0^+ &= I\, Q_0' + I'\, Q_1' \\ Q_1^+ &= I\, Q_0 + I'\, Q_1' \\ Z &= Q_0'\, Q_1' + Q_0\, Q_1 \end{aligned}$$

a. (**5 points**) As a consultant, your first job is to impress the managers of the company to make them feel good about hiring you. In order to do that you must quickly answer the following questions:

   (a) What type of state machine is this one (Mealy or Moore)?

   (b) How many states the finite machine has?

   (c) How many flip-flops does the machine uses?

   (d) What is the cost of the implementation of the combinatorial portion of the machine? Assume that the input's complement is available, and that the cost in the technology used is proportional to the number of inputs in the combinatorial gates.

b. (**5 points**) Now you need to show that there is some system to your method. Thus you need to build the state transition table based on the equations. Draw the state transition and output table for the machine.

c. (**10 points**) To actually earn your high consultancy fees, you must deliver something! Thus you must find ways to simplify the design. Having graduated from CMPUT329, the main tools in your toolbox are: state minimization, state assignment, and logis minization. Use them all to earn your pay! Compute the cost of the combinatorial part of your final solution.

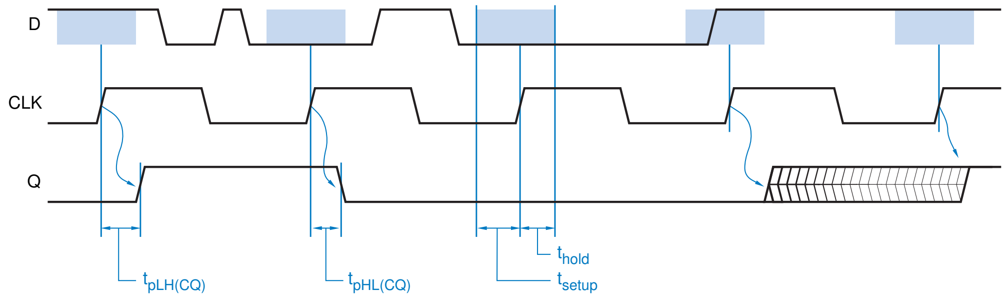


Figure 5: Timing Behaviour of a positive-edge flip-flop.

Question 5 (20 points): Memories, Hazards, Clock Skews

This is a **true** or **false** question. For each statement you have to indicate whether the statement is true or false. Use the capital letter **T** to indicate true, and the capital letter **F** to indicate false. You win 4 points for each correct answer. **You lose 2 points for each incorrect answer.** You are neither rewarded nor penalized for questions that you do not answer. If you answer all items correctly you will make a maximum of 20 points in this question. Regardless of how many items you answer wrong, your score in this question cannot be below zero.

a. (   ) Figure 5 shows the timing behavior of a positive-edge-triggered D flip-flop. When we build a finite state machine with that figure, the maximum clock cycle that we can have to ensure proper behavior of the flip-flops is given by the following equation:

$$ClockPeriod = t_{\text{setup}} + t_{\text{hold}} + t_{\text{seq}} + t_{\text{skew}}$$

where t_{seq} is the maximum sequential delay in the sequential logic of the machine and t_{skew} is the maximum clock skew.

b. (   ) To prevent fighting in a three state line, it is important that transitions into high impedance occur faster than transitions out of the high impedance state.

c. (   ) Although the organization of memory cells into a two-dimensional structure increases the number and the size of the gates required to implement the address decoders, a two-dimensional organization is still preferred because it reduces the number of external pins in each memory chip.

d. (   ) A Programmable Logic Array (PLA) contains a two-level structure of AND and OR gates. The connections between these gates are programmable by the user.

e. (   ) The write operation to a DRAM memory cell is destructive because they remove all the energy that was stored in the memory cell. Nonetheless the simple design of this cell makes it attractive for the high levels of integration required for high density memories.